What is claimed is:-

1. A tuning circuit comprising:

a first reactance,

a second reactance, and

an insulated gate field effect transistor having a gate arranged to receive a control signal, the first reactance being connected between the source of the field effect transistor and a first node and the second reactance having the same value as the first reactance and being connected between the drain of the field effect transistor and a second node,

wherein the first and second nodes are arranged so as to experience a balanced ac signal.

2. A circuit according to claim 1, wherein the first and second reactances are capacitors.

3. A circuit according to claim 1, wherein the first and second reactances are inductors.

4. A circuit according to claim 1, including a capacitor connected between said nodes.

5. A circuit according to claim 1, including an inductor connected between said nodes.

6. An insulated gate field effect transistor comprising:

source and drain regions within a surrounding region, and

gate electrode means provided over a channel or channels between said source and drain regions and over at least part of the boundary between said source and drain regions and said surrounding region, said surrounding region being provided with ground connection means for connection to an AC ground.

7. An insulated gate field effect transistor according to claim 6, wherein said ground connection means comprises a plurality of interconnected ohmic contacts to said surrounding region.

8. An insulated gate field effect transistor according to claim 6, wherein said gate electrode means encompasses said source and drain regions.

9. An insulated gate field effect transistor according to claim 6, wherein said source and drain regions are in a finger structure arrangement.

10. An insulated gate field effect transistor according to claim 6, wherein said source and drain regions are in a waffle structure arrangement.

11. An insulated gate field effect transistor according to claim 6, including a plurality of source and drain regions and an interconnection layer in which said source regions are connected together and said drain regions are connected together, the conductor or conductors of the interconnection layer being connected to said source and drain regions by splaying conductive paths.

12. An insulated gate field effect transistor according to claim 11, wherein said source and drain regions are in a waffle structure arrangement.

13. An insulated gate field effect transistor according to claim 12, wherein the interconnection layer comprises a source interconnection structure and a drain interconnection structure, said structures comprising respective sets of fingers extending diagonally, with respect to said waffle structure arrangement, which are interdigitated.

14. A tuning circuit comprising:

a first reactance,

a second reactance, and

an insulated gate field effect transistor having a gate arranged to receive a control signal,

the first reactance being connected between the source of the field effect transistor and a first node and the second reactance having the same value as the first reactance and being connected between the drain of the field effect transistor and a second node,

wherein

the first and second nodes are arranged so as to experience a balanced ac signal, and

the insulated gate field effect transistor comprises source and drain regions within a surrounding region and gate electrode means provided over a channel or channels between said source and drain regions and over at least part of the boundary between said source and drain regions and said surrounding region, said surrounding region being provided with ground connection means for connection to an AC ground.

15. A tuning circuit according to claim 14, wherein said ground connection means comprises a plurality of interconnected ohmic contacts to said surrounding region.

16. A tuning circuit according to claim 14, wherein said gate electrode means encompasses said source and drain regions.

17. A tuning circuit according to claim 14, wherein said source and drain regions are in a finger structure arrangement.

18. A tuning circuit according to claim 14, wherein said source and drain regions are in a waffle structure arrangement.

19. A tuning circuit according to claim 14, including a plurality of source and drain regions and an interconnection layer in which said source regions are connected together and said drain regions are connected together, the conductor or conductors of the interconnection layer being connected to said source and drain regions by splaying conductive paths.

20. A tuning circuit according to claim 19, wherein said source and drain regions are in a waffle structure arrangement.

21. A tuning circuit according to claim 20, wherein the interconnection layer comprises a source interconnection structure and a drain interconnection structure, said structures comprising respective sets of fingers extending diagonally, with respect to said waffle structure arrangement, which are interdigitated.

22. A tuning circuit according to claim 14, wherein the first and second reactances are capacitors.

23. A tuning circuit according to claim 14, wherein the first and second reactances are inductors.

24. A tuning circuit according to claim 14, including a capacitor connected between said nodes.

25. A tuning circuit according to claim 14 including an inductor connected between said nodes.

26. A resonant circuit including a tuning circuit, the tuning circuit comprising:

a first reactance,

a second reactance, and

an insulated gate field effect transistor having a gate arranged to receive a control signal,

the first reactance being connected between the source of the field effect transistor and a first node and the second reactance having the same value as the first reactance and being connected between the drain of the field effect transistor and a second node,

wherein

the first and second nodes are arranged so as to experience a balanced ac signal, and

the insulated gate field effect transistor comprises source and drain regions within a surrounding region and gate electrode means provided over a channel or channels between said source and drain regions and over at least part of the boundary between said source and drain regions and said surrounding region, said surrounding region being provided with ground connection means for connection to an AC ground.

27. A resonant circuit according to claim 26, wherein said ground connection means comprises a plurality of interconnected ohmic contacts to said surrounding region.

28. A resonant circuit according to claim 26, wherein said gate electrode means encompasses said source and drain regions.

29. A resonant circuit according to claim 26, wherein said source and drain regions are in a finger structure arrangement.

30. A resonant circuit according to claim 26, wherein said source and drain regions are in a waffle structure arrangement.

31. A resonant circuit according to claim 26, including a plurality of source and drain regions and an interconnection layer in which said source regions are connected together and said drain regions are connected together, the conductor or conductors of the interconnection layer being connected to said source and drain regions by splaying conductive paths.

32. A resonant circuit according to claim 31, wherein said source and drain regions are in a waffle structure arrangement.

33. A resonant circuit according to claim 32, wherein the interconnection layer comprises a source interconnection structure and a drain interconnection structure, said structures comprising respective sets of fingers extending diagonally, with respect to said waffle structure arrangement, which are interdigitated.

34. A resonant circuit according to claim 26, wherein the first and second reactances are capacitors.

35. A resonant circuit according to claim 26 wherein the first and second reactances are inductors.

36. A resonant circuit according to claim 26, including a capacitor connected between said nodes.

37. A resonant circuit according to claim 26 including an inductor connected between said nodes.

38. A resonant circuit according to claim 26, comprising an oscillator.

39. A resonant circuit according to claim 26, comprising a filter.

40. An insulated gate field effect transistor comprising a plurality of source and drain regions and an interconnection layer in which said source regions are connected together and said drain regions are connected together, the conductor or conductors of the interconnection layer being connected to said source and drain regions by splaying conductive paths.

41. An insulated gate field effect transistor according to claim 40, wherein said source and drain regions are in a waffle structure arrangement.

42. An insulated gate field effect transistor according to claim 41, wherein the interconnection layer comprises a source interconnection structure and a drain interconnection structure, said structures comprising respective sets of fingers extending diagonally, with respect to said waffle structure arrangement, which are interdigitated.